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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/905,356	08/04/97	BELGARD R	RAB-97-002

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EXAMINER	
NGUYEN, T	
ART UNIT	**PAPER NUMBER**
2751	8

DATE MAILED: 02/01/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/905,356	Belgard R.
Examiner	**Group Art Unit**
T Nguyen	2751

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 11-27-98.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 38-112 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 38-112 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s)._____

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other_____

Office Action Summary

DETAILED ACTION

Response to Amendment

1. This is a response to the amendment, filed 11/27/98.

2. Claims 38-112 are pending. Claims 82-112 has been added. Claims 1-5 have been canceled.

3. The submitted abstract is acceptable.

4. The rejections to claims 38-42 under 35 U.S.C. 112, first paragraph, as withdrawn in view of Applicant's amendment to overcome the 112 rejection.

Response to Arguments

5. Applicant's arguments with respect to claims 38-112 have been considered but are moot in view of the new ground(s) of rejection. After careful examination of the claims and their scope, the Examiner has made new art rejections to the claims due to their large breadth of scope.

Claim Rejections - 35 U.S.C. § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

7. Claims 38-112 are rejected under 35 U.S.C. 102(e) as being anticipated by Toy(US 4,400,774).

As to claims 38,43,49,77,89,92,95,98,101,104,107,110:

Toy discloses a cache addressing arrangement in a segmented computer system which stores a subset of the least significant real address bits obtained by translation of a previous virtual address and uses this subset in subsequent cache accessing operations(Abstract). Toy teaches the means for generating an actual physical address from a virtual address in a time period T, by calculating a linear address based on the virtual address and calculating the actual physical address based on the calculated linear address as address translation buffer(ATB 102)(Figure 1). The ATB inherently generates a linear address and physical address based on the virtual address, which comprises segment, page, word address information(Abstract, col 1 lns 20-31, col 3 lns 58-102). He teaches a fast physical address generator for generating a fast physical address related to the virtual address in a time < T as cache address unit 125, which generates a speculative address faster than the completion of the generation of the actual physical address(Figure 1, Abstract, col 3 lns 54-col 4 lns 36).

As to claims 39,44,50,58,62:

The fast/speculative address can be used to access the memory faster than the actual physical address(Abstract).

As to claims 40,45,51,59,63,67,71,79,83,84,88:

Toy teaches determining whether the fast physical address can be referenced and canceling the memory reference if the fast physical address and the actual physical address are different(col 5 lns 13-49).

As to claims 41,46,52,55,68,72,91,97,103,109:

Toy teaches generating the fast physical address based on the virtual address and partial linear address information by using the virtual address and a subset of the least significant real address bits obtained by translation of a previous virtual address to generate speculative addresses(Abstract).

As to claims 42,47,64,69,73,75,76,78,81:

He teaches a fast physical address generator for generating a fast physical address faster than the completion of the generation of the actual linear and physical addresses(Figure 1, Abstract, col 3 lns 54-col 4 lns 36).

As to claims 48,53,56,65:

Toy teaches generating the fast physical address based on some of the virtual address information and partial physical address information by using the virtual address and a subset of the least significant real address bits obtained by translation of a previous virtual address to generate speculative addresses(Abstract).

As to claim 60:

Toy teaches that the fast physical address comprises portion of the page frame that was from a prior physical address information and inherently the offset information from the segment information of the last virtual address(Abstract, col 1 lns 30-31, col 3 ln 54-col 4 lns 36).

As to claims 54,57,61,66,70,80,86,87:

Toy discloses a cache addressing arrangement in a segmented computer system which stores a subset of the least significant real address bits obtained by translation of a previous virtual address and uses this subset in subsequent cache accessing operations(Abstract). Toy stores portion of a physical address of a previous translation and using that information with a virtual address to generate speculative addresses(Abstract). Toy inherently teaches generating a linear address based on a virtual address because he teaches the ATB 102 to generate the physical address based on virtual address information(Abstract, col 1 lns 20-31, col 3 lns 58-102), which inherently comprises generating an intermediate linear address. He teaches a fast physical address generator for generating a fast physical address as cache address unit 125, which generates a speculative address faster than the generation of the actual physical address(Figure 1, Abstract, col 3 lns 54-col 4 lns 36). The fast/speculative physical address can be used to reference the memory.

As to claims 74:

Toy discloses a cache addressing arrangement in a segmented computer system which stores a subset of the least significant real address bits obtained by translation of a previous virtual address and uses this subset in subsequent cache accessing operations(Abstract). Toy stores portion of a physical address of a previous translation and using that information with a virtual address to

generate speculative addresses(Abstract). Toy inherently teaches generating a linear address based on a virtual address because he teaches the ATB 102 to generate the physical address based on virtual address information(Abstract, col 1 lns 20-31, col 3 lns 58-102), which inherently comprises generating an intermediate linear address. He teaches a fast physical address generator for generating a fast physical address as cache address unit 125, which generates a speculative address faster than the generation of the actual physical address(Figure 1, Abstract, col 3 lns 54-col 4 lns 36). The fast physical address can be used to reference the memory. Toy teaches canceling the memory reference if the fast physical address and the actual physical address are different(col 5 lns 13-49).

As to claims 82:

Toy discloses a cache addressing arrangement in a segmented computer system which stores a subset of the least significant real address bits obtained by translation of a previous virtual address and uses this subset in subsequent cache accessing operations(Abstract). Toy teaches the means for generating an actual physical address from a virtual address, by calculating a linear address based on the virtual address and calculating the actual physical address based on the calculated linear address as address translation buffer(ATB 102)(Figure 1). The ATB inherently generates a linear address and physical address based on the virtual address, which comprises segment, page, word address information(Abstract, col 1 lns 20-31, col 3 lns 58-102). He teaches a fast physical address generator for generating a fast physical address related to the virtual address as cache address unit 125, which generates a speculative address faster than the completion of the

generation of the actual physical address(Figure 1, Abstract, col 3 lns 54-col 4 lns 36). The bus interface circuit for initiating a fast memory access to a memory subsystem is taught as process 101, which initiates the memory access(Figure 1).

As to claims 85,93,99,105,111:

Toy teaches performing an actual memory reference after the fast memory reference is canceled(col 5 lns 13-49).

As to claims 90,96,102,108:

Toy discloses the comparator for determining whether the second address translation can be used for a memory access as comparator 109(col 5 lns 13-49).

As to claims 94,100,106,112:

Toy discloses a register for storing address information of previous virtual address(col 4 lns 25-37).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is (703) 305-3866.

9. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Than Nguyen
January 19, 1999

EDDIE P. CHAN
SUPERVISORY PATENT EXAMINER